Features

- Incorporates the ARM7TDMI ™ ARM® Thumb® Processor
  - Embedded ICE In-circuit Emulation, Debug Communication Channel Support
- 96K Bytes of Internal High-speed SRAM
- 256K Bytes of Internal High-speed ROM Integrating Default Boot Program
  - Downloads Application from External Storage Medium in Internal SRAM
- Double Master Memory Controller (DMMC)
  - Memory Protection Unit, Abort Status and Misalignment Detection
- Clock Generator and Power Management Controller (PMC)
  - 3 to 20 MHz and 32 kHz On-chip Oscillators with Two PLLs
  - Programmable Software Power Optimization Capabilities
  - Four Programmable External Clock Signals
- Advanced Interrupt Controller (AIC)
  - Thirty Individually Maskable, Eight-level Priority, Vectored Interrupt Sources
  - Seven External Interrupt Sources and One Fast Interrupt Source, Spurious Interrupt Protected
- Two 32-bit Parallel Input/Output Controllers (PIO) PIOA and PIOB
  - Sixty-three Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os
  - Input Change Interrupt Capability on Each I/O Line
  - Individually Programmable Open-drain and Synchronous Output
- System Timer (ST) Including a 16-bit Counter, Watchdog and Second Counter
- Real Time Clock (RTC) with Alarm Interrupt
- Debug Unit (DBGU), 2-wire USART and Support for Debug Communication Channel
  - Programmable ICE Access Prevention
- Twenty Peripheral Data Controller (PDC) Channels
- USB 1.1 Device Port (UDP)
  - Six Endpoints, On-chip Transceiver
  - 2K Bytes Configurable FIFO for Loading and Storing Messages
- Multimedia Card Interface (MCI)
  - Automatic Protocol Control and Fast Automatic Data Transfers with PDC
  - MMC and SDCard Compliant, Support for up to two SDCards
- Three Synchronous Serial Controllers (SSC)
  - Independent Clock and Frame Sync Signals for Each Receiver and Transmitter
  - AC97 and I²S Analog Interface Support, Time Division Multiplex Support
  - High-speed Continuous Data Stream Capabilities with 32-bit Data Transfer
- Four Universal Synchronous/Asynchronous Receiver Transmitters (USART)
  - Individual Baud Rate Generator
  - Support for ISO7816 T0/T1 Smart Card, Hardware and Software Handshaking, RS485 Support
  - Modem Control Lines on USART 1, IrDA Infrared Modulation/Demodulation
- Master/Slave Serial Peripheral Interface (SPI)
  - 8- to 16-bit Programmable Data Length
  - Four External Peripheral Chip Selects
- Two Three-channel 16-bit Timer/Counters (TC)
  - Three External Clock Inputs, Two multi-purpose I/O Pins per Channel
  - Double PWM Generation, Capture/Waveform Mode, Up/Down Capability
- Two-wire Interface (TWI)
  - Master Mode Support, All Two-wire Atmel EEPROM's Supported
- IEEE 1149.1 JTAG Boundary Scan on All Digital Pins
- Required Power Supplies:
  - 1.65V to 1.95V for VDDCORE, VDDOSC and VDDPLL
  - 1.65V to 3.6V on VDDIO
- Fully Static Operation: 0 Hz to 66 MHz @2.7V/1.8V, up to 60 MIPS
- Available in a 100-lead LQFP Package

ARM7TDMI™ - based Microcontroller

AT91RM3400 Summary

Rev. 1790D–ATARM–23-May-02

Description

The AT91RM3400 is a fully integrated member of the Atmel advanced AT91 ARM microcontroller family. Having no external memory interface and equipped with embedded SRAM and ROM, it is ideal for numerous applications with medium memory requirements but which demand high performance.

Several options are available to download software to the internal SRAM. These include downloading from a serial EEPROM or serial DataFlash® or downloading through the USB Device Port. Additionally, customizing of the embedded ROM is available on request for large volume opportunities.

The Advanced Interrupt Controller (AIC) enhances the interrupt handling performance of the ARM7TDMI processor by providing multiple vectored, prioritized interrupt sources and reduces the cycles taken to transfer to an interrupt handler.

The Peripheral Data Controller (PDC) provides DMA channels for all the serial peripherals, enabling them to transfer data to or from on-chip memories without processor intervention. This reduces the processor overhead when dealing with transfers of continuous data streams.

The set of Parallel I/O (PIO) controllers multiplex the peripheral input/output lines with general purpose data I/Os, reducing the external pin count of the device and providing an interrupt and open drain capability on each line.

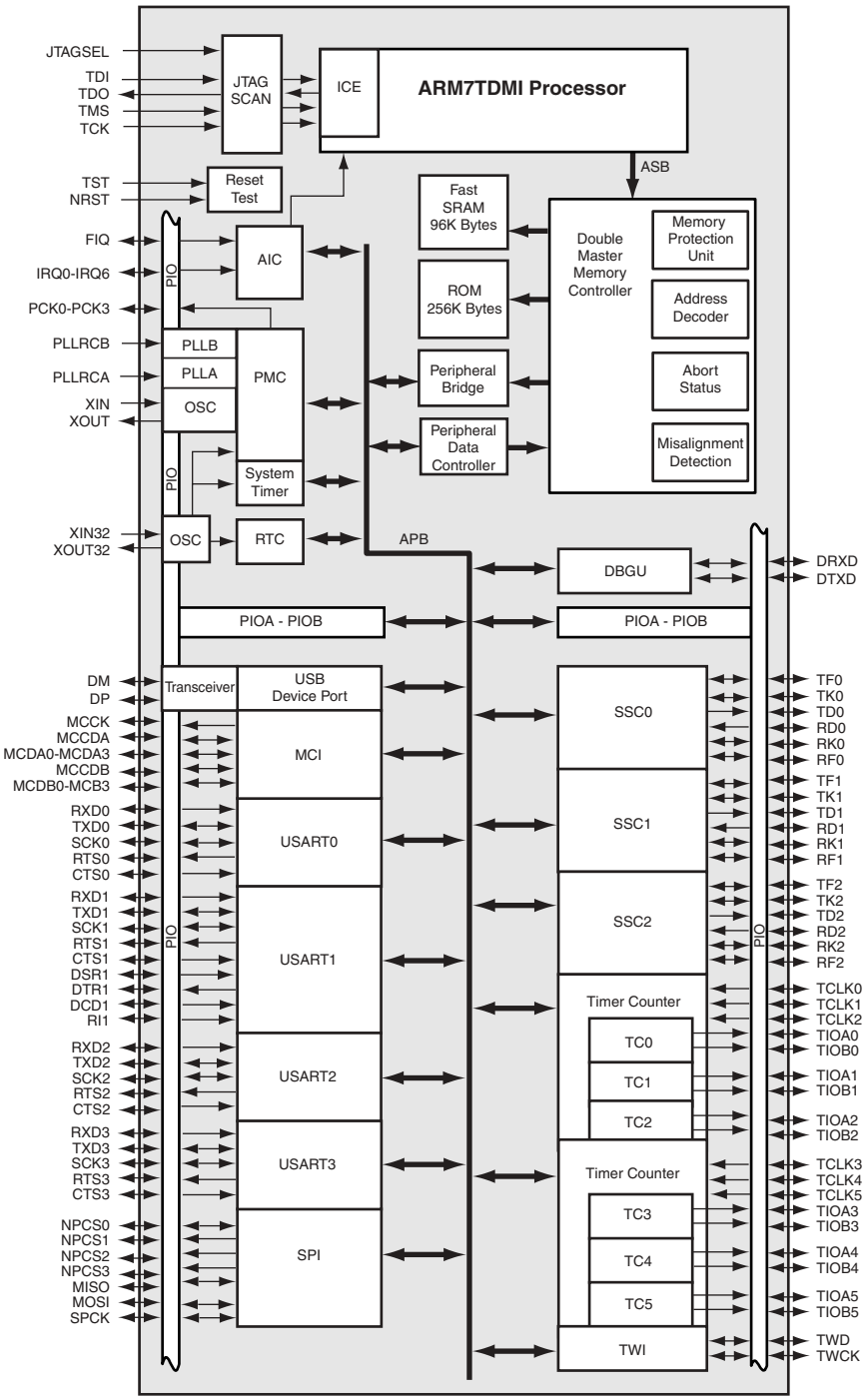
The Power Management Controller (PMC) keeps system power consumption to a minimum by selectively enabling and/or disabling the core and various peripherals under software control. It uses an enhanced clock generator to provide a selection of clock signals including a slow clock (32 kHz) for power-saving mode.

The wide range of system interfaces includes USB V1.1 Device, Multimedia Card, Serial Peripheral Interface (SPI) and Two-wire Interface (TWI). Peripherals include multiple USARTs, Timer/Counters and Serial Synchronous Controllers (SSC).

The AT91RM3400 includes an extensive set of peripherals that operate in accordance with several industry standards, such as those used in audio, communication, computer and smart card applications.

Block Diagram

Figure 1. AT91RM3400 Block Description

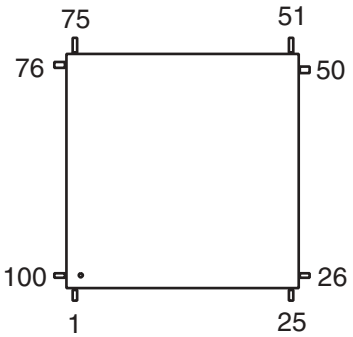


Pin Configuration

Table 1. AT91RM3400 Pinout in 100-lead LQFP Package

1	VDDCORE	26	PA11	51	PA30	76	PB21
2	GND	27	PA12	52	PA31	77	PB22
3	VDDPLL	28	PA13	53	PB0	78	JTAGSEL
4	PLLRCB	29	VDDIO	54	PB1	79	TDI
5	GNDPLL	30	GND	55	PB2	80	TDO
6	XOUT	31	PA14	56	PB3	81	TCK
7	XIN	32	PA15	57	PB4	82	TMS
8	VDDOSC	33	PA16	58	PB5	83	VDDIO
9	GNDOSC	34	PA17	59	PB6	84	GND
10	XOUT32	35	VDDCORE	60	PB7	85	TST
11	XIN32	36	GND	61	PB8	86	NRST
12	VDDPLL	37	PA18	62	PB9	87	VDDCORE
13	PLLRCA	38	PA19	63	PB10	88	GND
14	GNDPLL	39	PA20	64	PB11	89	PB23
15	PA0	40	PA21	65	PB12	90	PB24
16	PA1	41	PA22	66	VDDIO	91	PB25
17	PA2	42	PA23	67	GND	92	PB26
18	PA3	43	PA24	68	PB13	93	PB27
19	PA4	44	PA25	69	PB14	94	PB28
20	PA5	45	PA26	70	PB15	95	PB29
21	PA6	46	PA27	71	PB16	96	PB30
22	PA7	47	PA28	72	PB17	97	DM
23	PA8	48	VDDIO	73	PB18	98	DP
24	PA9	49	GND	74	PB19	99	VDDIO
25	PA10	50	PA29	75	PB20	100	GND

Figure 2. Pin Configuration in 100-lead LQFP Package (Top View)



Peripheral Multiplexing on PIO Lines

Table 2. Definition of Pin Multiplexing for AT91RM3400

PIO Controller A		
I/O Line	**Peripheral A**	**Peripheral B**
PA0	MISO	–
PA1	MOSI	–
PA2	SPCK	PCK0
PA3	NPCS0	PCK1
PA4	NPCS1	USUSPEND(1)
PA5	NPCS2	SCK1
PA6	NPCS3	SCK2
PA7	TWD	PCK2
PA8	TWCK	PCK3
PA9	TXD0	–
PA10	RXD0	UTXOEN(1)
PA11	SCK0	TCLK0
PA12	CTS0	TCLK1
PA13	RTS0	TCLK2
PA14	RXD1	–
PA15	TXD1	–
PA16	RTS1	TIOA0
PA17	CTS1	TIOB0
PA18	DTR1	TIOA1
PA19	DSR1	TIOB1
PA20	DCD1	TIOA2
PA21	RI1	TIOB2
PA22	RXD2	URXD(1)
PA23	TXD2	UTXD(1)
PA24	MCCK	RTS0
PA25	MCCDA	RTS1
PA26	MCDA0	
PA27	MCDA1	UEON(1)
PA28	MCDA2	RTS2
PA29	MCDA3	CTS2
PA30	DRXD	–
PA31	DTXD	–

PIO Controller B		
I/O Line	**Peripheral A**	**Peripheral B**
PB0	TF0	TIOB3
PB1	TK0	TCLK3
PB2	TD0	RTS2
PB3	RD0	RTS3
PB4	RK0	PCK0
PB5	RF0	TIOA3
PB6	TF1	TIOB4
PB7	TK1	TCLK4
PB8	TD1	NPCS1
PB9	RD1	NPCS2
PB10	RK1	PCK1
PB11	RF1	TIOA4
PB12	TF2	TIOB5
PB13	TK2	TCLK5
PB14	TD2	NPCS3
PB15	RD2	PCK1
PB16	RK2	PCK2
PB17	RF2	TIOA5
PB18	RTS3	MCCDB
PB19	CTS3	MCDB0
PB20	TXD3	DTR1
PB21	RXD3	
PB22	SCK3	PCK3
PB23	FIQ	
PB24	IRQ0	TD0
PB25	IRQ1	TD1
PB26	IRQ2	TD2
PB27	IRQ3	DTXD
PB28	IRQ4	MCDB1
PB29	IRQ5	MCDB2
PB30	IRQ6	MCDB3

Note: 1. USB Transceiver Interface

Pin Description

Table 3. Pin Description for the AT91RM3400

Pin Name	Function	Type	Active Level	Comments
Power				
VDDIO	Memory I/O Lines Power Supply	Power		1.65V to 3.6V
VDDPLL	Oscillator and PLL Power Supply	Power		1.65V to 1.95V
VDDCORE	Core Chip Power Supply	Power		1.65V to 1.95V
VDDOSC	Oscillator Power Supply	Power		1.65V to 1.95V
GND	Ground	Ground		
GNDPLL	PLL Ground	Ground		
GNDOSC	Oscillator Ground	Ground		
Power Management (PMC)				
XIN	Main Crystal Input	Input		
XOUT	Main Crystal Output	Output		
XIN32	32KHz Crystal Input	Input		
XOUT32	32KHz Crystal Output	Output		
PLLRCA	PLL A Filter	Input		
PLLRCB	PLL B Filter	Input		
PCK0 - PCK3	Programmable Clock Output	Output		
ICE and JTAG				
TCK	Test Clock	Input		
TDI	Test Data In	Input		
TDO	Test Data Out	Output		
TMS	Test Mode Select	Input		
JTAGSEL	JTAG Selection	Input		
Reset/Test				
NRST	Microcontroller Reset	Input	Low	No on-chip pull-up
TST	Test Mode Select	Input		Must be tied low for normal operation
Debug Unit				
DRXD	Debug Receive Data	Input		
DTXD	Debug Transmit Data	Output		
AIC				
IRQ0 - IRQ6	Interrupt Inputs	Input		
FIQ	Fast Interrupt Input	Input		
PIO				

Table 3. Pin Description for the AT91RM3400 (Continued)

Pin Name	Function	Type	Active Level	Comments
PA0 - PA31	Parallel IO Controller A	I/O		Pulled-up input at reset
PB0 - PB30	Parallel IO Controller B	I/O		Pulled-up input at reset
Multi-media Card Interface				
MCCK	Multimedia Card Clock	Output		
MCCDA	Multimedia Card A Command	I/O		
MCDA0 - MCDA3	Multimedia Card A Data	I/O		
MCCDB	Multimedia Card B Command	I/O		
MCDB0 - MCDB3	Multimedia Card B Data	I/O		
USART				
SCK0 - SCK3	Serial Clock	I/O		
TXD0 - TXD3	Transmit Data	I/O		
RXD0 - RXD3	Receive Data	Input		
RTS0 - RTS3	Ready To Send	Output		
CTS0 - CTS3	Clear To Send	Input		
DSR1	Data Set Ready	Input		
DTR1	Data Terminal Ready	Output		
DCD1	Data Carrier Detect	Input		
RI1	Ring Indicator	Input		
USB Device Port				
DDM	USB Device Port Data -	Analog		
DDP	USB Device Port Data +	Analog		
Synchronous Serial Controller				
TD0 - TD2	Transmit Data	Output		
RD0 - RD2	Receive Data	Input		
TK0 - TK2	Transmit Clock	I/O		
RK0 - RK2	Receive Clock	I/O		
TF0 - TF2	Transmit Frame Sync	I/O		
RF0 - RF2	Receive Frame Sync	I/O		
Timer/Counter				
TCLK0 - TCLK5	External Clock Input	Input		
TIOA0 - TIOA5	Multipurpose Timer I/O Pin A	I/O		
TIOB0 - TIOB5	Multipurpose Timer I/O Pin B	I/O		
SPI				
MISO	Master In Slave Out	I/O		
MOSI	Master Out Slave In	I/O		
SPCK	SPI Serial Clock	I/O		

Table 3. Pin Description for the AT91RM3400 (Continued)

Pin Name	Function	Type	Active Level	Comments
NPCS0 - NPCS3	SPI Peripheral Chip Select 0	I/O	Low	
Two-wire Interface				
TWD	Two-wire Serial Data	I/O		
TWCK	Two-wire Serial Clock	I/O		

Associated Documentation

Table 4. Documentation Applicable to the AT91RM3400 Product

Block	Document Title	Owner	Literature Number
ARM7TDMI System	ARM7TDMI (Rev 4)Technical Reference Manual	ARM Ltd.	DD10210A
	Double Master Memory Controller Datasheet	Atmel	1760
	Peripheral Data Controller 2 Datasheet	Atmel	1734
	Boot ROM Datasheet	Atmel	1791
System Peripherals	Advanced Interrupt Controller 2 Datasheet	Atmel	1796
	Advanced Power Management Controller for ARM7 Datasheet	Atmel	2636
	System Timer Datasheet	Atmel	1763
	Real Time Clock 2 Datasheet	Atmel	1245
	Parallel IO Controller 2 Datasheet	Atmel	1725
	Debug Unit Datasheet	Atmel	1754
User Peripherals	USB Device Port Datasheet	Atmel	1765
	Multimedia Card Interface Datasheet	Atmel	1764
	Synchronous Serial Controller Datasheet	Atmel	1762
	USART 3 Datasheet	Atmel	1739
	Serial Peripheral Interface Datasheet	Atmel	1244
	Two-wire Interface Datasheet	Atmel	1761
	Timer Counter Datasheet	Atmel	1753

Product Overview

Power Supplies

The AT91RM3400 has four types of power supply pins:

- VDDCORE pins power the chip core and must be between 1.65V and 1.95V, 1.8V nominal.
- VDDIO pins power the I/O lines and must be between 1.65V and 3.6V, 1.8V, 3V or 3.3V nominal
- VDDPLL pins power the PLL cells and must be between 1.65V and 1.95V, 1.8V nominal
- VDDOSC pin powers both oscillators and must be between 1.65V and 1.95V, 1.8V nominal

Ground pins are common for all power supplies except the VDDPLL and VDDOSC, for which the GNDPLL and the GNDOSC pins are provided respectively.

Powering VDDIO with a voltage lower than 3V prevents any use of the USB Device Port.

Input/Output Considerations

The AT91RM3400 pins support VDDIO + 0.4V as maximum voltage. All PIO pins (multiplexed or non-multiplexed) integrate a programmable pull-up resistor of about 100 kΩ. As soon as the NRST reset line is asserted, outputs are disabled and all pull-up resistors are enabled. By doing so, the AT91RM3400 guarantees that the tri-state inputs are held in a valid logic level and no oscillations are produced inside the device, thereby preventing excess power consumption.

Reset

Reset restores the default states of the user interface registers, as defined in the user interface of each peripheral, and forces the ARM7TDMI to perform the next instruction fetch from address zero. Except for the program counter and the Current Program Status Register, the ARM7TDMI registers do not have defined reset states. Reset state also deactivates all internal clocks to prevent any power consumption.

NRST Pin

NRST is an active low reset input. It is asserted asynchronously, but exit from reset is internally synchronized to the Slow Clock (SLCK). At power-up, NRST must be active until the on-chip oscillator is stable. During normal operation, in order to insure correct initialization, NRST must be active for a minimum of one slow clock cycle.

Watchdog Reset

The internally generated watchdog reset has the same effect as the NRST pin. However, the NRST pin has priority if both types of reset coincide.

Emulation and Test Functions

Test Pin

The AT91RM3400 has one dedicated pin to define the device operating mode. The device changes its operating mode as soon as the level on this pin changes, independently of any clock. The user must make sure that this pin is tied at low level to ensure normal operating conditions. Test Pin Operating Modes are defined below in Table 5:

Table 5. Operating Modes

TST	Operating Mode
0	Normal Operating Mode
1	Test Mode(1)

Note: 1. Test modes are not described in this document.

Embedded In-circuit Emulator

ARM standard embedded In-circuit Emulation is supported via the JTAG/ICE port. It is connected to a host computer via an ICE Interface. Embedded ICE mode is selected when JTAGSEL is low. It is not possible to switch directly between ICE and JTAG operations. A chip reset must be performed (NRST) after JTAGSEL is changed.

IEEE 1149.1 JTAG Boundary Scan

The IEEE 1149.1 JTAG Boundary Scan is enabled when JTAGSEL is high. The SAMPLE, EXTEST and BYPASS functions are implemented. In ICE Debug mode, the ARM core responds with a non-JTAG chip ID that identifies the core to the ICE system. This is not IEEE 1149.1 JTAG compliant.

Note: It is not possible to switch directly between JTAG and ICE operations. A chip reset must be performed (NRST) after JTAGSEL is changed.

Automatic Wake-up on Debug Request

The user software can program the Power Management Controller to enter Idle Mode, in which the core clock is stopped to save power. However, when the AT91RM3400 is in Idle Mode, a debug request cannot be processed, as the core clock must be active to enter the Debug Mode. In order to resolve this, the Power Management Controller automatically re-enables the core clock as soon as a debug request is received.

For further details of the Power Management Controller, see the Power Management Controller datasheet referenced in Table 4 on page 9.

Clock and Power Saving Features

The AT91RM3400 is clocked by several programmable clock signals provided by the Clock Generator, which is controlled through the Power Management Controller. The following clock signals are to be considered as within the AT91RM3400:

- Slow Clock (SLCK), 32768 Hz typical frequency, provided specifically for the System Timer and the Real Time Clock, is considered to be the only permanent clock signal of the AT91RM3400
- MCK, the Master Clock, programmable frequency between a few hertz and maximum operating speed, feeding the ARM7TDMI, the Double Master Memory Controller and all the peripherals
- USBCK, the USB Clock, programmable frequency (typically 48 MHz)
- PCK0 - PCK3, programmable output clock signals

The AT91RM3400 also features Idle Mode and Peripheral Clock Control, allowing the user to optimize the power consumption of the system as a function of the application requirements.

Double Master Memory Controller

The AT91RM3400 features a Double Master Memory Controller to manage the Internal Advanced System Bus and arbitrate the accesses required by the ARM7TDMI core and the Peripheral Data Controller. It is composed of the following features:

- A Bus Arbiter, arbitrates the PDC and the ARM7TDMI access requests.
- An Address Decoder, splits the 4G byte address space in areas to access SRAM, ROM and the embedded peripherals. The external memory areas are not used in the AT91RM3400.
- An Abort Status, traces the source and the cause of errors during access to the Double Master Memory Controller.
- A Misaligned Access Detector, detects when either the PDC or the ARM7TDMI provides an address which is not consistent with the kind of access required.
- A Memory Protection Unit, defines up to 16 areas, each configurable to prevent access in write or in user mode. Base addresses of the areas are programmable up to bit 21 only and their sizes are programmable between 1K bytes and 1M bytes. The Memory Protection Unit also permits the protection of the peripheral address space.

Internal SRAM

The AT91RM3400 embeds a 96-Kbyte SRAM bank, which is mapped on the Internal Memory Area 2 of the Double Master Memory Controller. After the reset and until Remap Command is performed, the SRAM is only accessible at address 0x0020 0000. After the Remap, the SRAM also becomes available at address 0x0.

Internal ROM

The AT91RM3400 features one bank of 256K bytes of ROM that is mapped into the Internal Memory Area 1 of the Double Master Memory Controller. At all times, the ROM is mapped at address 0x0010 0000. It is also accessible at address 0x0 after the reset and before the Remap Command.

Peripherals

The AT91RM3400 integrates several peripherals, which are classified as system or user peripherals.

All embedded peripherals are 32-bit accessible by the Peripheral Bridge, and can be programmed with a minimum number of instructions. The peripheral register set is composed of control, mode, data, status and enable/disable/status registers.

An on-chip Peripheral Data Controller (PDC) transfers data between the embedded peripherals and on- and off-chip memory address space without processor intervention. Most importantly, the 20 PDC channels remove the processor interrupt handling overhead, making it possible to transfer up to 64K continuous words (8-, 16- or 32-bit) just by defining the start address and the size, thus increasing the performance of the AT91RM3400, and reducing power consumption.

Peripheral Identifiers

Each embedded user peripheral and the PIO controllers have an identifier between 2 and 31, which corresponds to its interrupt source number and its peripheral clock control number. Identifier 0 is reserved for the FIQ. The Identifier 1 is used for one single interrupt source, asserted by one of the system peripherals. Table 6 on page 14 details the peripheral identifiers.

Table 6. Peripheral Identifiers

Peripheral ID	Peripheral Mnemonic	Peripheral Name	External Interrupt
0	AIC	Advanced Interrupt Controller	FIQ
1	PMC	Power Management Controller	
	ST	System Timer	
	RTC	Real Time Clock	
	DBGU	Debug Unit	
2	PIOA	Parallel IO Controller A	
3	PIOB	Parallel IO Controller B	
4	–	Reserved	
5	–	Reserved	
6	US0	USART 0	
7	US1	USART 1	
8	US2	USART 2	
9	US3	USART 3	
10	MCI	Multimedia Card Interface	
11	UDP	USB Device Port	
12	TWI	Two-Wire Interface	
13	SPI	Serial Peripheral Interface	
14	SSC0	Serial Synchronous Controller 0	
15	SSC1	Serial Synchronous Controller 1	
16	SSC2	Serial Synchronous Controller 2	
17	TC0	Timer Counter 0	
18	TC1	Timer Counter 1	
19	TC2	Timer Counter 2	
20	TC3	Timer Counter 3	
21	TC4	Timer Counter 4	
22	TC5	Timer Counter 5	
23	–	Reserved	
24	–	Reserved	
25	AIC	Advanced Interrupt Controller	IRQ0
26	AIC	Advanced Interrupt Controller	IRQ1
27	AIC	Advanced Interrupt Controller	IRQ2
28	AIC	Advanced Interrupt Controller	IRQ3
29	AIC	Advanced Interrupt Controller	IRQ4
30	AIC	Advanced Interrupt Controller	IRQ5
31	AIC	Advanced Interrupt Controller	IRQ6

Peripheral User Interface

Peripheral Access

The AT91RM3400 peripherals are connected to a 32-bit wide Advanced Peripheral Bus. Peripheral registers are only word accessible. Byte and half-word accesses are not supported. If a byte or a half-word access is attempted, the double master memory controller automatically masks the lowest address bits and generates a word access.

Each User Peripheral has a 16-Kbyte address space allocated.

The System Peripherals are all mapped in the 4K bytes highest address space, between addresses 0xFFFF F000 and 0xFFFF FFFF. Each peripheral has an address space of 256 or 512 bytes, representing 64 or 128 registers

Peripheral Registers

The following register definitions are common to all peripherals:

- Control Register: Write-only register that triggers a command when a one is written to the corresponding position at the appropriate address. Writing a zero has no effect.
- Mode Register: Read/Write register that defines the configuration of the peripheral. Usually has a value of 0x0 after a reset.
- Data Registers: Read/Write register that enables the exchange of data between the processor and the peripheral.
- Status Register: Read-only register that returns the status of the peripheral.
- Enable/Disable/Status Registers are shadow command registers. Writing a one in the Enable Register sets the corresponding bit in the Status Register. Writing a one in the Disable Register resets the corresponding bit and the result can be read in the Status Register. Writing a bit to zero has no effect. This register access method maximizes the efficiency of bit manipulation, and enables modification of a register with a single non-interruptible instruction, replacing the costly read-modify-write operation.

Unused bits in the peripheral registers are shown as “–” and must be written at 0 for upward compatibility. These bits read 0.

Peripheral Interrupt Control

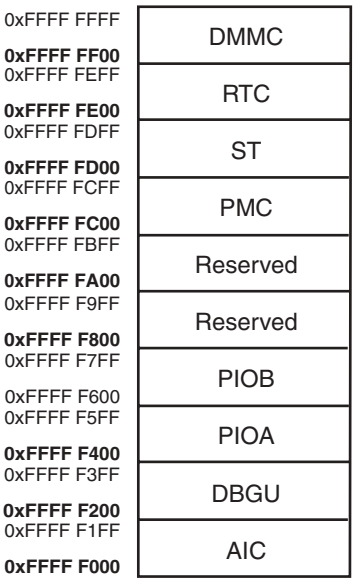
The Interrupt Control of each peripheral is controlled from the status register using the interrupt mask. The status register bits are ANDed to their corresponding interrupt mask bits and the result is then ORed to generate the Interrupt Source signal to the Advanced Interrupt Controller.

The interrupt mask is read in the Interrupt Mask Register and is modified with the Interrupt Enable Register and the Interrupt Disable Register. The enable/disable/status (or mask) makes it possible to enable or disable peripheral interrupt sources with a non-interruptible single instruction. This eliminates the need for interrupt masking at the AIC or Core level in real-time and multi-tasking systems.

Peripheral Mapping

System Peripheral Mapping

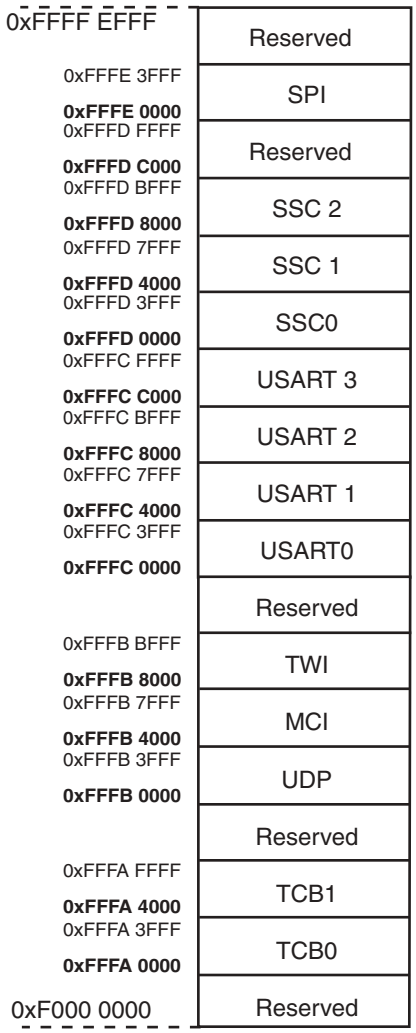
Figure 3. System Peripheral Map



Address	Peripheral	Peripheral Name	Size
0xFFFF FFFF **0xFFFF FF00**	DMMC	Double Master Memory Controller	256 Bytes/64 Words
0xFFFF FEFF **0xFFFF FE00**	RTC	Real Time Clock	256 Bytes/64Words
0xFFFF FDFF **0xFFFF FD00**	ST	System Timer	256 Bytes/64Words
0xFFFF FCFF **0xFFFF FC00**	PMC	Power Management Controller	256 Bytes/64Words
0xFFFF FBFF **0xFFFF FA00**	Reserved		512 Bytes/128Words
0xFFFF F9FF **0xFFFF F800**	Reserved		512 Bytes/128Words
0xFFFF F7FF 0xFFFF F600	PIOB	Parallel IO Controller B	512 Bytes/128Words
0xFFFF F5FF **0xFFFF F400**	PIOA	Parallel IO Controller A	512 Bytes/128Words
0xFFFF F3FF **0xFFFF F200**	DBGU	Debug Unit	512 Bytes/128Words
0xFFFF F1FF **0xFFFF F000**	AIC	Advanced Interrupt Controller	512 Bytes/128Words

User Peripheral Mapping

Figure 4. User Peripheral Map



Peripheral Data Controller

The AT91RM3400 has a 20-channel Peripheral Data Controller dedicated to the following peripherals:

- Debug Unit
- Four on-chip USARTs,
- SPI
- Three SSCs
- Multimedia Card Interface.

One PDC channel is connected to the receiver and one to the transmitter of each peripheral requiring a high data throughput.

Peripheral Data Controller User Interface

The user interfaces (programming registers and status control bits) of all the PDC channels are integrated into the user interface of the peripheral to which they are assigned.

Each PDC channel is made up of:

- One 32-bit current buffer pointer register
- One 16-bit current buffer counter register
- One 32-bit next buffer pointer register
- One 16-bit next buffer counter register
- Two Control Bits enable and/or disable the channel
- One Enable Status Bit showing the activity
- One Transfer Trigger coming from the peripheral
- One Buffer Full Status Bit in the Status Register of the Peripheral
- One Buffer Empty Status Bit in the Status Register of the Peripheral

Peripheral Data Controller Operations

The current pointer and counter registers typically write the address and the size of the buffer, and, when read, show the next transfer address and the remaining transfer numbers. When a transfer is performed, the address is incremented and the counter decrements.

The next transfer pointer and counter registers permit frames to be chained easily, thus preventing requirement for fast interrupt latency while handling the transfers or consecutive data frames. When the current counter reaches 0 and the next counter is not null, the next counter and pointer are loaded in the current registers, thus allowing a permanent transfer rate.

The control bit permits the triggers from the PDC to be enabled and disabled in order to read the pointer and counter registers safely without any risk of their changing between both reads. Each PDC channel must be enabled before being used.

Two status bits indicating the end of the current buffers, and the end of both the current and next buffers, are directly mapped in the peripheral status register and can trigger an interrupt request to the AIC.

Priority of PDC Transfer Requests

The PDC handles the transfer requests from the PDC channels according to the following priorities.

- If requests are simultaneous, they are treated in the following sequence:
  - Debug Unit receiver
  - USART receivers
  - SSC receivers
  - MCI receiver
  - SPI receiver
  - Debug Unit transmitter
  - USART transmitters
  - SSC transmitters
  - MCI transmitter
  - SPI transmitter
- If transfer requests are not simultaneous, they are treated in the order they occurred, but requests from the receivers are handled first and then followed by requests from the transmitters.

For further details on the Peripheral Data Controller, see the Peripheral Data Controller datasheet referenced in Table 4 on page 9.

System Peripherals

Power Management Controller

The AT91RM3400 Power Management Controller (PMC) implements the Idle Mode (ARM7TDMI core clock stopped until the next interrupt) and enables the user to adapt the power consumption of the system to the application requirements (independent peripheral clock control). It also controls the activity and provides programming parameters for the Clock Generator elements, the main oscillator and the PLLs.

It furnishes the Slow Clock (SLCK), the Processor Clock (PCK), the Master Clock (MCK), the USB Clock (USBCK) and the Programmable Clock Outputs (PCK0 to PCK3). The Master Clock does not integrate the additional divider, i.e., the Processor Clock is based on the Master Clock.

For further details on the Power Management Controller, refer to the Power Management Controller datasheet referenced in Table 4 on page 9.

System Timer

The System Timer integrates three different free-running timers:

- A Period Interval Timer sets the base time for an Operating System.
- A Watchdog Timer built around a 16-bit counter is used to prevent system lock-up if the software becomes trapped in a deadlock. It can generate an internal reset or an interrupt.
- A Real-time Timer counts elapsed seconds.

These timers count forwards or backwards using the Slow Clock provided by the Power Management Controller. Typically, this clock has a frequency of 32768 Hz.

For additional information on the System Timer, refer to the System Timer datasheet referenced in Table 4 on page 9.

Real-time Clock

The Real-time Clock (RTC) peripheral is designed for very low power consumption. It combines a complete time-of-day clock with alarm and a two hundred-year Gregorian calendar, complemented by a programmable periodic interrupt.

The time and calendar values are coded in binary-coded decimal (BCD) format. The time format can be 24-hour mode or 12-hour mode with an AM/PM indicator.

Updating time and calendar fields and configuring the alarm fields is performed by a parallel capture on the 32-bit data bus. An entry control is performed to avoid loading registers with incompatible BCD format data or with an incompatible date according to the current month/year/century.

Additional details on the Real Time Clock are contained in the Real Time Clock datasheet referenced in Table 4 on page 9.

Advanced Interrupt Controller

The AT91RM3400 features an 8-level priority, individually maskable, vectored interrupt controller. This feature substantially reduces the software and real-time overhead in handling internal and external interrupts.

The interrupt controller is connected to the NFIQ (fast interrupt request) and the NIRQ (standard interrupt request) inputs of the ARM7TDMI processor. The NIRQ line can be asserted by the interrupts generated by the on-chip peripherals and the external interrupt request lines: IRQ0 to IRQ6. The processor's NFIQ line can normally be asserted only by the external fast interrupt request input: FIQ and the Fast Forcing feature permit redirecting any interrupt source onto the NFIQ.

Internal sources are programmed to be level sensitive or edge triggered. External sources can be programmed to be positive or negative edge triggered or high or low-level sensitive.

For further details on the Advanced Interrupt Controller and interrupt handling, refer to the Advanced Interrupt Controller datasheet referenced in Table 4 on page 9 and Table 6 on page 14, “Peripheral Identifiers”.

Parallel I/O Controllers

The AT91RM3400 is equipped with two Parallel I/O Controllers, PIOA and PIOB, that control respectively 32 I/O lines and 31 I/O lines.

Each I/O line can be assigned up to two embedded peripherals as defined in the I/O Line Multiplexing table in Table 2 on page 5. Otherwise, each I/O line can be used as general purpose input or output.

In all cases, the user can on each individual pin perform the following tasks:

- Read the level on the pin.
- Enable and input change interrupt.
- Configure the pin in open-drain (driven low only)
- Enable a pull-up resistor of about 100kΩ on the pin.

When the pins are defined as a general-purpose output, the user can define a mask which changes (set or clear) the levels of pins on the same PIO Controller in one write instruction.

For additional information on the Parallel I/O Controller Refer to the Parallel I/O Controller datasheet referenced in Table 4 on page 9.

Note: The information relating to the “peripheral loop” in the document referred to above does not apply to the AT91RM3400.

Debug Unit

The Debug Unit provides a serial interface compatible with the USART, but bonding out only the RXD and TXD pins. These pins are named DRXD and DTXD. A Baud Rate Generator permits the selection of the communication speed and serial asynchronous full duplex data flow. CPU Overhead requirements are reduced by the addition of two PDC channels.

The Debug Unit also grants the interrupt handling of the COMMTX and COMMRX signals coming from the ARM7TDMI ICE Breaker and traces the activity of the Debug Communication Channel.

Moreover, the Debug Unit integrates two Chip ID registers which contain a unique number for each device of the family. This feature permits the identification of the architecture of the device, and, additionally, the set of embedded peripherals, the size of the internal memories and the silicon revision, thus facilitating tracing the evolution of the products.

Finally, the Debug Unit has a special register to assert the NTRST signal of the ARM Core ICE interface. This enables the software to permit or to forbid any system access through the JTAG. In the first revision of the AT91RM3400, this feature is disabled (and therefore the JTAG enabled) after the reset.

For further details on the Debug Unit and the corresponding interrupt handling, refer to the Debug Unit datasheet referenced in Table 4 on page 9.

User Peripherals

USB Device Port

The AT91RM3400 USB Device Port provides a high speed full-duplex serial communication port at a baud rate of 12 Mbits/s. It can be connected to a USB host or a USB Hub in the USB "tiered start" topology.

It includes the following features:

- USB 1.1 compliant. Can operate at a baud rate of 12 Mbits/s
- On-Chip USB bus transceiver on pins DM and DP.
- One Dual Port RAM of 2048 bytes accessible in byte mode only as an Internal Memory
- Programmable endpoint types with support for 6 control, interrupt, bulk or isochronous endpoints
- Independent interrupt for each endpoint, start-of-frame, reset, suspend and resume events
- Ping-pong transaction supported

Each endpoint can support all types of transfers. A type is suggested according to the fixed size of the DPR allocated to this endpoint:

- Endpoint 0: 8 bytes (suggested type: control transfers)
- Endpoint 1: 64 bytes (supports ping-pong, suggested type: bulk transfers)
- Endpoint 2: 64 bytes (supports ping-pong, suggested type: bulk transfers)
- Endpoint 3: 8 bytes (suggested type: interrupt transfers)
- Endpoint 4: 256 bytes (supports ping-pong, suggested type: isochronous transfers)
- Endpoint 5: 256 bytes (supports ping-pong, suggested type: isochronous transfers)

The USB protocol uses differential signaling between the DM and DP pins for half-duplex data transmission. A 1.5 KΩ pull-up resistor is required to be connected to the USB cable's D+ signal to pull the DP pin high when not driven.

For further details on the USB Device Port, refer to the USB Device Port datasheet referenced in Table 4 on page 9.

Multimedia Card Interface

The Multimedia Card Interface supports the MultiMediaCard (MMC) Specification v2.2 and the SD Memory Card Specification v1.0. It can operate at up to Master Clock divided by 2 and supports interfacing up to 16 slots. Each slot may be used to interface with a MultiMediaCard Bus (up to 30 Cards) or with an SD Memory Card. Only one slot can be selected at a time (slots are multiplexed).

The MCI provides a command register, response registers, data registers, time-out counters and error detection logic which automatically handle the transmission of commands and the reception of the associated responses and data with a limited CPU overhead. It supports stream, block and multi-block data read and write. It is linked to the PDC making CPU intervention unnecessary for large buffer transfers.

As an energy-saving feature, the MCI is equipped with embedded power management to slowdown the clock rate when not being used.

For further details on the Multimedia Card Interface, see the Multimedia Card Interface datasheet referenced in Table 4 on page 9.

Synchronous Serial Controller

The Synchronous Serial Controller supports many serial synchronous communication protocols generally used in the audio and telecom applications such as I²S, AC97, Short Frame Sync, Long Frame Sync, etc.

The SSC contains an independent receiver and transmitter and a common clock divider. The receiver and the transmitter each interface with three signals: the TD/RD signal for the data, the TK/RK signal for the clock and the TF/RF signal for the Frame Sync.

Transfers contain up to 16 data items of up to 32 bits. They can be programmed to start automatically or on different events detected on the Frame Sync signal. The SSC's high-level of programmability and its two dedicated PDC channels of up to 32 bits permit a continuous high bit rate data transfer without software intervention.

Featuring connection to two PDC channels, the SSC permits interfacing with low CPU over- head, for example, to the following:

- CODECs in master or slave modes
- DAC through dedicated serial interface, particularly the I2S
- AC97 V2.1 protocol
- Magnetic card reader
- Time Division Multiplexed Buses
- Printer and scanner interface
- SPI used in full or half duplex, in master or slave modes with one chip select only

For further details on the Serial Synchronous Controller, see the Serial Synchronous Controller datasheet referenced in Table 4 on page 9.

Universal Synchronous/ Asynchronous Receiver/ Transmitter

The AT91RM3400 provides two identical, full-duplex, universal synchronous/asynchronous receiver/transmitters that interface to the APB and are connected to the Peripheral Data Controller.

The main features are:

- Programmable baud rate generator with external or internal clock, as well as slow clock
- Parity, framing and overrun error detection
- Line break generation and detection
- Automatic echo, local loop back and remote loop back channel modes
- Multi-drop mode: address detection and generation
- Two dedicated peripheral data controller channels
- 5-, 6-, 7-, 8- and 9-bit character length generation, delay timing and pulse-width modulation.

All USARTs support ISO7816 Smart Card T0 or T1 protocols and manage 2 signals, RTS and CTS, allowing hardware handshaking.

All USARTs also feature an operating mode supporting the modulation and demodulation IrDA in SIR (Slow Infrared) at up to 115200 baud.

The USART 1 has a complete set of modem signals (RTS/CTS/DSR/DTR/DCD/RI). Outputs can be controlled directly from the USART User Interface and inputs can generate an USART interrupt when changing state.

For further details on the USART, refer to the USART datasheets in Table 4 on page 9.

Serial Peripheral Interface

The AT91RM3400 includes an SPI that provides communication with external devices in master or slave mode.

In master mode, the SPI has four external independently-programmable peripheral chip select lines that can be connected to up to four devices without external components or 15 devices via an external decoder. The data length is programmable from 8- to 16-bits, MSB or LSB first, with programmable polarity and phase, and can operate to access at full speed only one peripheral or to communicate through the same buffer with many peripherals. Speed and bit stream delays are fully configurable and independently definable for each chip select.

In slave mode, the NPCS0 pin can be used as a slave select input (NSS).

The two PDC channels connected to the SPI allow fast and low CPU overhead communication with serial peripherals.

For further details on the Serial Peripheral Interface, see the Serial Peripheral Interface datasheet referenced in Table 4 on page 9.

Two-wire Interface

The Two-wire Interface (TWI) interconnects components on a unique two-wire bus made up of one clock line and one data line with speeds of up to 400 Kbits based on a byte-oriented transfer format. It can be used with any Atmel two-wire bus serial EEPROM. The TWI is programmable as a master or a slave with sequential or single-byte access. Multiple master capability is supported. Arbitration of the bus is performed internally and turns the TWI into slave mode automatically if the bus arbitration is lost.

A configurable baud rate generator permits adaptation of the output data rate to a wide range of clock frequencies.

For additional details on the Two-wire Interface, refer to the Two-wire Interface datasheet referenced in Table 4 on page 9.

Timer/Counter

The AT91RM3400 features two Timer/Counter blocks, each containing three identical 16-bit Timer/Counter channels. Each channel can be independently programmed to perform a wide range of functions including frequency measurement, event counting, interval measurement, pulse generation, delay timing and pulse-width modulation.

Each Timer/Counter channel has 3 external clock inputs (TCLK), 5 internal clock inputs, and 2 multi-purpose input/output signals (TIOA/TIOB) that can be configured by the user. Each channel drives an internal interrupt signal that can be programmed to generate processor interrupts via the AIC (Advanced Interrupt Controller).

The Timer/Counter block has two global registers that act upon all three TC channels. The Block Control Register allows the three channels to be started simultaneously with the same instruction. The Block Mode Register defines the external clock inputs for each Timer/Counter channel, allowing them to be chained.

Each Timer/Counter block operates independently and has a complete set of block and channel registers.

In Waveform Mode, each Timer Counter supports double waves generation or single waveform generation on TIOA with trigger on input TIOB. Up and down counting are supported and 3 compare registers are available. Outputs can be configured to be set, cleared or toggled on trigger or compare events. Interrupts can be generated for any event.

In Capture Mode, 2 load and 1 compare registers are available. Triggers and inputs event detection are largely programmable and load events can generate interrupts, stop the operations or disable the channel clock.

For added details on the Timer/Counter Interface, refer to the Timer/Counter Interface datasheet referenced in Table 4 on page 9.

Package Drawing

Figure 5. 100-lead LQFP Package Drawing

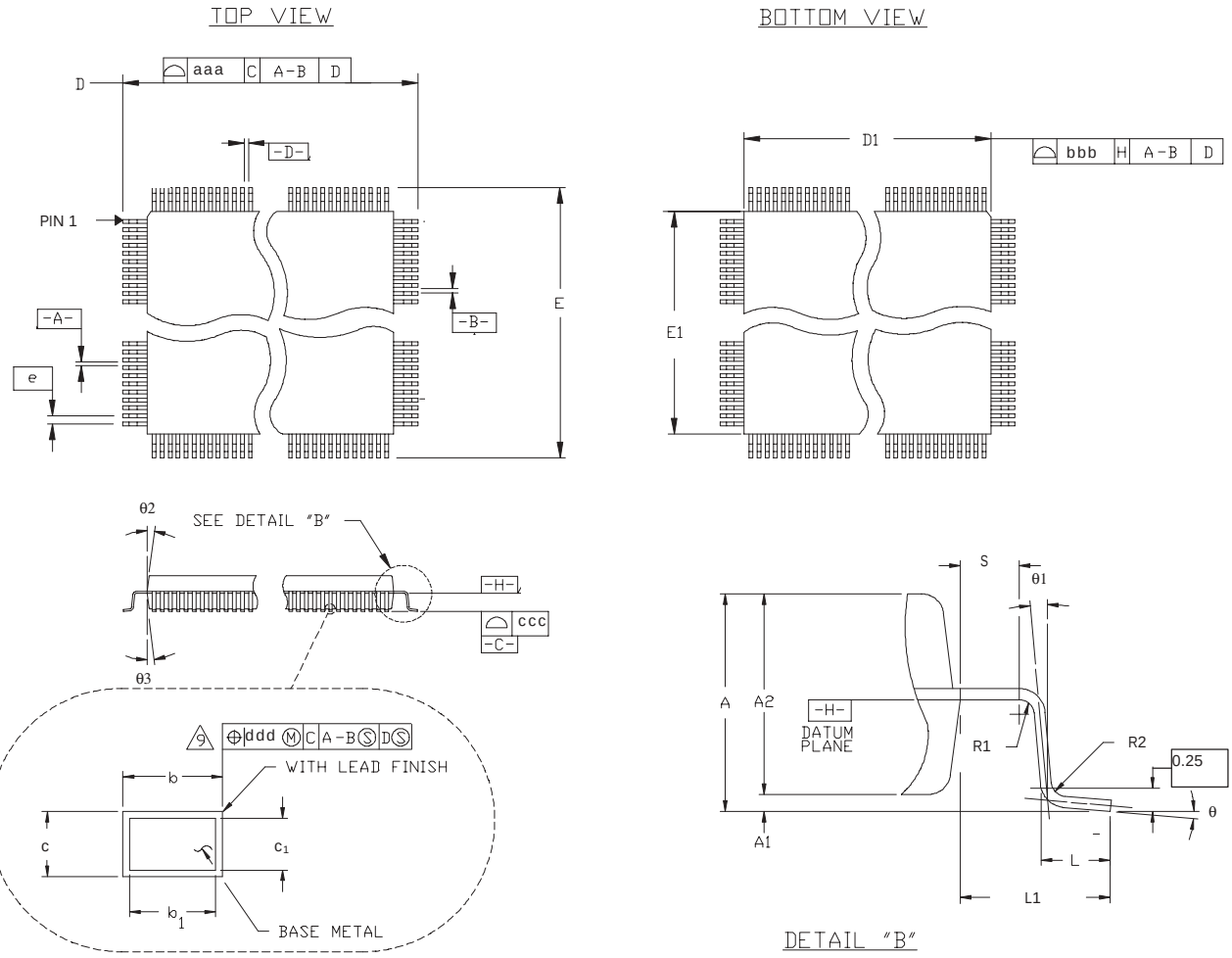


Table 7. 100-lead LQFP Package Dimensions (in mm)

Symbol	Min	Typ	Max
c	0.09		0.2
c1	0.09		0.16
L	0.45	0.6	0.75
L1		1.00 REF	
R2	0.08		0.2
R1	0.08		
S	0.2		
Θ	0°	3.5°	7°
Θ1	0°		
Θ2	11°	12°	13°
Θ3	11°	12°	13°
A			1.6
A1	0.05		0.15
A2	1.35	1.4	1.45
Tolerances of Form and Position			
aaa		0.2	
bbb		0.2	

Table 8. Lead Count Dimensions (mm)

Pin Count	D/E BSC	D1/E1 BSC	b			b1			e BSC	ccc	ddd
			Min	Typ	Max	Min	Typ	Max			
100	16.0	14.0	0.17	0.22	0.27	0.17	0.2	0.23	0.50	0.10	0.06

Table 9. Device and 100-lead LQFP Package Maximum Weight

TBD	mg

Soldering Profile

Table 10 gives the recommended soldering profile from J-STD-20.

Table 10. Soldering Profile

	Convection or IR/Convection	VPR
Average Ramp-up Rate (183°C to Peak)	3°C/sec. max.	10°C/sec.
Preheat Temperature 125°C ±25°C	120 sec. max	
Temperature Maintained Above 183°C	60 sec. to 150 sec.	
Time within 5°C of Actual Peak Temperature	10 sec. to 20 sec.	60 sec.
Peak Temperature Range	220 +5/-0°C or 235 +5/-0°C	215 to 219°C or 235 +5/-0°C
Ramp-down Rate	6°C/sec.	10°C/sec.
Time 25°C to Peak Temperature	6 min. max	

Small packages may be subject to higher temperatures if they are reflowed in boards with larger components. In this case, small packages may have to withstand temperatures of up to 235°C, not 220°C (IR reflow).

Recommended package reflow conditions depend on package thickness and volume. See Table 11.

Table 11. Recommended Package Reflow Conditions (1, 2, 3)

Parameter	Temperature
Convection	235 +5/-0°C
VPR	235 +5/-0°C
IR/Convection	235 +5/-0°C

When certain small thin packages are used on boards without larger packages, these small packages may be classified at 220°C instead of 235°C.

Notes:
1. The packages are qualified by Atmel by using IR reflow conditions, not convection or VPR.
2. By default, the package level 1 is qualified at 220°C (unless 235°C is stipulated).
3. The body temperature is the most important parameter but other profile parameters such as total exposure time to hot temperature or heating rate may also influence component reliability.

A maximum of three reflow passes is allowed per component.

Document Details

Title	AT91RM3400 Summary
Literature Number	1790

Revision History

Version A	**Publication Date:** September 2001
Version B	**Publication Date:** October 2001
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Revisions Since Previous Version

Page: 10	NRST Pin paragraph changed.
Page: 11	IEEE 1149.1 JTAG Boundary Scan paragraph changed.
Page: 27	Added Table 8: Lead Count Dimensions.
Page: 27	Added Table 9: Device and Package Maximum Weight.
Page: 28	Section added: Soldering Profile.
Page: 28	Added Table 10: Soldering Profile
Page: 28	Added Table 11: Recommended Package Reflow Condition

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